Code: 20IT3402

II B.Tech - II Semester – Regular / Supplementary Examinations MAY - 2023

COMPUTER ORGANIZATION (INFORMATION TECHNOLOGY)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.

2. All parts of Question must be answered in one place.

| | | | BL | СО | Max. | | | | |
|----|--------|--|----|-----|-------|--|--|--|--|
| | | | | | Marks | | | | |
| | UNIT-I | | | | | | | | |
| 1 | a) | Explain the process of bus construction with | L2 | CO1 | 7 M | | | | |
| | | multiplexers. | | | | | | | |
| | b) | Discuss different Micro Operations with | L2 | CO2 | 7 M | | | | |
| | | suitable examples. | | | | | | | |
| OR | | | | | | | | | |
| 2 | a) | Discuss about register transfer, bus and | L2 | CO1 | 7 M | | | | |
| | | memory transfer. | | | | | | | |
| | b) | The following transfer statements specify a | L2 | CO2 | 7 M | | | | |
| | | memory. Explain the memory operation in | | | | | | | |
| | | each case | | | | | | | |
| | | i) $R2 \leftarrow M[AR]$ | | | | | | | |
| | | ii) $M[AR] \leftarrow R3$ | | | | | | | |
| | | iii) $R5 \leftarrow M[R5]$ | | | | | | | |

| UNIT-II | | | | | | | | |
|----------|----|--|----|-----|------|--|--|--|
| 3 | a) | Explain about the Instruction Cycle. | L2 | CO1 | 7 M | | | |
| | b) | Draw a flowchart for interrupt cycle and | L3 | CO2 | 7 M | | | |
| | | explain with an example. | | | | | | |
| OR | | | | | | | | |
| 4 | a) | Discuss about various Basic Instruction | L2 | CO1 | 7 M | | | |
| | | Formats with example. | | | | | | |
| | b) | Illustrate the input-output configuration with | L3 | CO2 | 7 M | | | |
| | | interrupts. | | | | | | |
| | | | | | | | | |
| UNIT-III | | | | | | | | |
| 5 | | Illustrate various Addressing Modes with | L3 | CO2 | 14 M | | | |
| | | suitable example. | | | | | | |
| | OR | | | | | | | |
| 6 | a) | Illustrate the Program interrupt with suitable | L3 | CO2 | 7 M | | | |
| | | example. | | | | | | |
| | b) | Interpret an arithmetic statement using three | L3 | CO3 | 7 M | | | |
| | | and two Addressing Instructions with your | | | | | | |
| | | own. | | | | | | |
| | | | | | | | | |
| UNIT-IV | | | | | | | | |
| 7 | a) | Illustrate the Booth Multiplication | L2 | CO2 | 10 M | | | |
| | | Algorithm with suitable example. | | | | | | |
| | b) | Analyze how Cache memory is faster in | L4 | CO4 | 4 M | | | |
| | | computing comparing with other memories. | | | | | | |
| | OR | | | | | | | |

| 8 | a) | Explain about Addition Algorithm with | L2 | CO3 | 7 M | | | |
|--------|----|--|----|-----|-----|--|--|--|
| | | suitable example. | | | | | | |
| | b) | Explain about Auxiliary memory and Main | L4 | CO4 | 7 M | | | |
| | | Memory . | | | | | | |
| | | | | | | | | |
| UNIT-V | | | | | | | | |
| 9 | a) | Explain asynchronous data transfer with | L4 | CO4 | 7 M | | | |
| | | Handshaking method . | | | | | | |
| | b) | Explain in detail about the Pros and Cons of | L4 | CO4 | 7 M | | | |
| | | Parallel Processing. | | | | | | |
| OR | | | | | | | | |
| 10 | a) | Explain in detail about Direct Memory | L4 | CO4 | 7 M | | | |
| | | Access with neat Sketch. | | | | | | |
| | b) | What is pipelining? Explain about | L4 | CO4 | 7 M | | | |
| | | Instruction Pipeline. | | | | | | |